IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Richard W. Foote, et al.
Serial No.:	10/777,012
Filed:	February 11, 2004
For:	SEMICONDUCTOR APPARATUS COMPRISING BIPOLAR TRANSISTORS AND METAL OXIDE SEMICONDUCTOR TRANSISTORS AND MANUFACTURING METHOD
Group No.:	2891
Examiner:	Steven J. Fulk

MAIL STOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request. This request is being filed with a notice of appeal.

STATUS OF THE CLAIMS

Claims 1-4, 7-10, 13-17, 17, and 20-21 remain pending in the application.

Claims 1-4, 7-10, 13-17, 17, and 20-21 have been rejected.

REMARKS

In Section 2 of the April 24, 2006 Advisory Action, the Examiner rejected Claims 1-4, 7-10, 13-17, 17, and 20-21 under 35 U.S.C. § 103(a) as obvious over US Patent 4,902,640 to Sachitano *et al.* ("*Sachitano*") in view of US Patent 6,441,441 to Suda ("*Suda*"). The Examiner further relies upon *Wolf* (NPL Reference "U") – of the prior art made of record and not relied upon – to provide motivation not found or suggested in either *Sachitano* or *Suda*, in an attempt to buttress his interpretations thereof.

The Applicant respectfully submits: i) that there is no suggestion or motivation – without the benefit of hindsight reconstruction from the present application – to selectively cull from and combine the reference teachings; and ii) that – even if one of **ordinary** skill in the art were so motivated - the proposed combination of *Sachitano* or *Suda*, in would not result in the invention as recited in independent Claim 1. As such, the Examiner has failed to establish a *prima facie* case of obviousness.

Independent Claim 1 is reproduced here for the convenience of the review panel:

> 1. A semiconductor apparatus comprising at least one double poly bipolar transistor and at least one double poly metal oxide semiconductor (MOS) transistor, wherein a base of the double poly bipolar transistor and a gate of the double poly metal oxide semiconductor transistor contain substantially identical dopants. (*Emphasis added*).

The Examiner has conceded that *Sachitano* does not teach or suggest a base of a double poly bipolar transistor and a gate of a double poly metal oxide semiconductor transistor containing substantially identical dopants, as required by independent Claim 1. Applicant agrees.

Applicant respectfully submits that one of ordinary skill, having only *Sachitano* before him, would not be prospectively moved to spontaneously assume that the substantial disclosure of *Sachitano* was in need of a base of a double poly bipolar transistor and a gate of a double poly metal oxide semiconductor transistor containing substantially identical dopants. In fact, Applicant respectfully submits that *Sachitano* appears to suggest differentiated doping during formation. (Col. 4, line 55 – Col. 5, line 7; Col. 10, lines 31-51).

In order to overcome these admitted deficiencies of *Sachitano*, the Examiner selectively culls from *Suda* the **inference** of a base of a double poly bipolar transistor and a gate of a double poly metal oxide semiconductor transistor containing substantially identical dopants – even though *Suda* itself does not explicitly teach that these two structures contain substantially identical dopants. The Examiner further ignores the fact that, in order to combine the references as suggested, one of ordinary skill in the art would have to completely overlook the remainder of *Suda's* various teachings of PMOS transistor and an NPN bipolar transistor structure and formation – teachings that vary significantly from *Sachitano's*.

The Examiner offers generally available knowledge, as allegedly shown in *Wolf*, as the motivation for one of ordinary skill in the art to embark on this speculative and selective combination process – even though neither *Sachitano* nor *Suda* appear to identify operation as a surface channel device or any particular degradation effects as a problem or concern.

In summary, there is neither a motivation nor a suggestion in either the cited references or the knowledge of a person of ordinary skill in the art at the time of the Applicant's invention to: 1)

spontaneously assume a deficiency in *Sachitano*; 2) seek out and find *Suda*; 3) ignore almost all of *Suda's* teachings of structure and process; 4) selectively cull a single concept from *Suda* – a double poly bipolar transistor and a gate of a double poly metal oxide semiconductor transistor containing substantially identical dopants – even though *Suda* does not explicitly disclose such; and 5) substantially modify the processes and structures of *Sachitano* to incorporate this spontaneous extraction of concept from *Suda*. Furthermore, even if the references were to be so selectively combined, the combination would still not result in the Applicant's invention as recited in independent Claim 1 of the Application.

As such, Claim 1 distinguishes over the improper hindsight combination of *Sachitano* and *Suda*, and the other art of reference. As a result, Claim 1 and dependent Claims 2-4, 7-10, 13-17, and 20-21 are all believed to be allowable.

For these reasons, the Applicant respectfully submits that the Examiner has failed to establish a *prima facie* case of obviousness and, without more, the Applicant is entitled to grant of a patent.

Respectfully submitted,

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